REMARKS

Favorable reconsideration of this application is respectfully requested in view of the following remarks. Claims 1-23 are pending in the present application.

Teleconference

The Examiner is respectfully thanked for the courtesies extended during the teleconference with the undersigned on October 7, 2003. Although the Examiner denied the request for a personal interview, the Examiner's time in speaking with the undersigned is appreciated. The bases for rejecting the interview request was that the case is under final and that a previous interview had been granted on this case. It should, however, be understood that the previous interview was conducted to discuss a rejection of the claims based upon a reference that differs from the currently cited rejections based upon the Van Doren document. Therefore, the undersigned has not had an opportunity to discuss the currently pending rejections with the Examiner in a personal interview. In addition, a previous request for an interview made during the time period set for reply to the Non-Final Office Action (June 10, 2003) was not granted because the Examiner was unable to find a Primary Examiner to attend the interview.

Claim Rejection Under 35 U.S.C. §103

The test for determining if a claim is rendered obvious by one or more references for purposes of a rejection under 35 U.S.C. § 103 is set forth in MPEP § 706.02(j):

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference

> (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claims 1-23 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over the disclosure contained in U.S. Patent No. 6,209,065 to Van Doren et al. ("Van Doren"). This rejection is respectfully traversed because Van Doren as modified in the manner suggested in the Official Action does not disclose the invention as claimed in Claims 1, 9, and 19 and the claims that depend therefrom. In addition, the Official Action has failed to meet the burden of proving a *prima facie* case of obviousness.

Van Doren discloses a mechanism for optimizing the generation of a commit-signal by control logic in response to a memory reference issued by a processor to a local node having a hierarchical switch for interconnecting a plurality of nodes. (Abstract). The mechanism includes a structure that indicates whether the memory operation affects other processors of other nodes. (Abstract). In addition, Van Doren discloses that the structure facilitates ordering at the local node as a means for reducing the latency of inter-reference ordering. (column3, lines 56-61, column 4, lines 1-3). Thus, Van Doren is directed to inter-reference ordering operations designed to increase "the efficiency of a shared memory multiprocessor system by relaxing the completion requirement" and "to improving the performance of a shared memory system by reducing the latency associated with memory barriers." (column 3, lines 38-44). In other words, Van Doren is directed to increasing efficiency by performing inter-reference ordering operations at the local nodes, which apparently reduces bandwidth usage during requests submitted by the processors.

Van Doren further discloses that "a cache coherence protocol is utilized to maintain consistency among the caches." (column 6, lines 13 and 14). In addition, Van Doren states

that if a processor has a shared ownership of a cache line, "it must inform the system and potentially invalidate data copies in other caches." (column 6, lines 27-30). Therefore, Van Doren discloses that a synchronization operation is performed between the processors to maintain cache coherence.

In contrast to the Van Doren disclosure, the present invention as set forth in Claims 1, 9, and 19 pertain to a method and systems for returning data from one processor or memory in a multi-processor system that does not include utilization of synchronous cache coherence protocols. Instead, the processors or memory in the multi-processor system of the present invention are operated in an asynchronous manner because the processors do not have to synchronize a response to a request for a data block. In other words, each of the processors process requests for a block of data independently. When a processor discovers it does not have the data block requested by another processor, it simply drops the request without responding. On the other hand, if the processor has the requested data block, it provides the requested block to the requesting processor.

The Official Action correctly notes that Van Doren fails to disclose that only the processor or shared memory having the valid copy responds to the request. The Official Action attempts to address this deficiency in Van Doren by asserting official notice that it is well known that a processor having ownership of the valid data provides the valid data. Applicants neither agree nor disagree with the position asserted in the Official Action. Instead, it is respectfully submitted that the Official Action has not shown how it concludes that a processor having ownership of the valid data providing the valid data is the same as "only the processor or shared memory having the valid copy responds to the request." It is further respectfully submitted that the Official Action has not set forth any arguments to indicate that Van Doren could be modified to disclose this element of the present invention.

In fact, the Official Action never directly addresses how Van Doren could be modified to include the feature that "only the processor or shared memory having the valid copy responds to the request." Instead, the Official Action states that "[i]t would have been obvious to one of ordinary skill in the memory art at the time the invention was made for the valid data to be provided to the requester by either the processor that modified the data or the main/shared memory because the processor that modified the data or the main/shared memory are the only sources for the valid data and official notice is taken thereof." Clearly, the modification of Van Doren proposed in the Official Action would not yield the present invention as set forth in Claims 1, 9, and 19. Instead, the Official Action merely states that the processor or the main/shared memory that modified the data are the only sources for the valid data. Accordingly, even assuming for the sake of argument that the proposed modification of Van Doren is proper, the Official Action has failed to meet the burden of setting forth a prima facie case of obviousness as the proposed modification of Van Doren fails to teach or suggest all the elements set forth in Claims 1, 9, and 19 of the present invention.

More particularly, the arguments asserted in the Official Action do not suggest that **only** the processor or shared memory having the valid copy responds to the request. In other words, the Official Action does not suggest that processors or the shared memory that do not have the valid copy do not respond to the request. Clearly, the processor or shared memory having the valid copy will respond to the request. However, what is not discussed in the Official Action is how the other processors and memory that have invalid copies of the data behave in response to requests for data. That is, there is no discussion in the Official Action of how the processors and memory that do not have the valid copy operate in response to the request for data.

The use of the term "only" in claim language is typically interpreted as a negative limitation and generally operates to exclude elements not contained in the claim. See, e.g., Lewmar Marine, Inc. v. Barient, Inc., 827 F.2d 749 (CAFC 1987). In addition, the term "'only'...may not be read out of the claim." Id. Accordingly, the Official Action erred in failing to address the term "only" contained in the claims.

Moreover, even assuming for the sake of argument that the motivation for modifying Van Doren as asserted in the Official Action were valid, such a proposed modification would not yield the present invention as set forth in Claims 1, 9, and 19. As stated hereinabove, the proposed modification would not include the element that "only the processor or memory having the valid copy of the data responds to the request." It is thus respectfully submitted that Van Doren does not render the present invention as set forth in Claims 1, 9, and 19 unpatentable.

In fact, Van Doren discloses the diametric opposite of the features claimed in Claims 1, 9, and 19. More particularly, Van Doren discloses that the processors having invalid copies also respond to the request for data. For example, in column 19, lines 9-11, Van Doren states that "[o]nce these [FrdMod and Inval] probes reach their destinations, ***each*** processor returns either the data or an acknowledgement back to the directory control logic 1415." (emphasis added). Therefore, Van Doren discloses that each of the processors responds to the request for data.

Based at least on the above-disclosure, it would not have been obvious to modify the Van Doren reference to include the feature that "only the processor or memory having the valid copy of the data responds to the request." As set forth in MPEP §2143.01, "[i]f the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed

modification." In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Clearly, in this situation, any proposed modification of Van Doren to enable it to read on the features set forth in Claims 1, 9, and 19 of the present invention would alter Van Doren in a manner that is unsatisfactory for its intended purpose. More particularly, Van Doren discloses that a cache coherence protocol involving the potential invalidation of copies in various caches or a synchronization operation, is performed where a processor does not have exclusive ownership of a cache line. (column 6, lines 27-30). In addition, because Van Doren also discloses that each of the processors respond to a request for data, the cache coherence protocol intended to be used in Van Doren would be negated. Accordingly, there is no suggestion or motivation to modify Van Doren to include the features set forth in Claims 1, 9 and 19 of the present invention.

Accordingly, the Examiner is respectfully requested to withdraw the rejection of Claims 1, 9, and 19 as being unpatentable over the disclosure contained in Van Doren, with or without the proposed modification set forth in the Official Action.

Claims 2-5, 7, 8, 10-18 and 20-23 depend from allowable Claims 1, 9, and 19 and are also allowable at least by virtue of their dependencies. These claims are also allowable as the elements contained therein are not disclosed in the Van Doren document.

For instance, Claim 6 of the present invention includes that the one or more processors and memory that receive a request for data have invalid copies of the requested data drop the request. The Official Action sets forth a rejection of Claim 6 as being unpatentable over the disclosure contained in column 7, lines 15-18 of the Van Doren document. It is respectfully submitted, however, that the above-cited section of the Van Doren document does not disclose at least this element.

The disclosure in column 7, lines 15-18 of Van Doren states, "[i]n response to the FrdMod probe, the dirty cache line is returned to the system and the dirty copy stored in the cache is invalidated." Thus, Van Doren discloses that the processors that receive the request and have invalid copies do not drop the request, but rather, return "the dirty cache line" to the system. This is in direct contrast with the elements set forth in Claim 6.

As another example, Claims 21-23 include that the valid copy is returned asynchronously. The term "asynchronous" is defined in the specification of the present application as a scheme where the processors in a multiprocessor system "do not have to synchronize a response to a request for a data block." (Specification, page 5, line 20-23). The Official Action cites to column 5, lines 63-67 and column 7, lines 63-65 of the Van Doren document as disclosing asynchronous responses to requests. These cited sections disclose the ability of the Van Doren invention to issue memory reference operations out-of-order. Issuance of memory reference operations out-of-order is not the same as not requiring a synchronization of a response to a request for a data block. Accordingly, the disclosure contained in Van Doren regarding out-of-order memory reference operations cannot render unpatentable the elements contained in Claims 21-23.

Response to Arguments

It is respectfully submitted that the Official Action has misconstrued the arguments set forth in the previous Response filed on June 17, 2003. Applicant did not state that "Van Doren fails to disclose how the processors and memory having invalid copies respond to the request of data" as asserted in the Official Action. Instead, Applicant stated that the previous Official Action failed to address how the processors and memory having invalid copies respond to data requests in Van Doren. Moreover, Applicant also stated that Van Doren

actually does disclose how the processors and memory having invalid copies respond to the data request. Namely, as stated in column 19, lines 9-11, Van Doren discloses that "each processor returns either the data or an acknowledgement back to the directory control logic 1415." Therefore, the Official Action has mischaracterized Applicant's position with respect to the disclosure contained in Van Doren.

The Official Action further argues that "maintaining coherency in a multiprocessor system...requires specific maintenance of the ownership of the data (such as the processor having the ownership and valid data responds to the request and other processors not having the valid data will not respond to the request), otherwise, the data becomes corrupt and the data within the system is no longer reliable." It is not at all clear as to how the Official Action arrives at its conclusion that processors that do not have the valid data "will not respond to the request." As discussed above, Van Doren states that all of the processors respond to the request with either the valid data or an acknowledgement. Thus, the acknowledgement constitutes a response that would not corrupt the data.

The crux of the arguments set forth in the Official Action are based upon the processor having the valid copy not only responding to the request, but sending the valid copy to the requestor. Again, it is important to note that the transmission of the valid copy from the processor that contains the valid copy to the requesting processor does not imply, in any respect, that processors that do not contain the valid copy do not respond to the request. There is absolutely nothing in the arguments presented in the Official Action to suggest that such an inference can logically be made.

In addition, the arguments are directed to invalidation operations, e.g., synchronization, and that caches having the invalid copies cannot respond to the requesting processor, somehow implies a dropping of the request does not have any logical bases. For

instance, Van Doren discloses that processors having dirty cache lines still respond to the request with an acknowledgement. (column 19, lines 9-11). Clearly, therefore, it is improper to conclude that synchronization operations result in dropping of requests by processors that do not have a valid copy of the requested data.

In addition, assuming for the sake of argument that the position identified above is valid, then there would be no need for the feature "in each of the processors and memory that receive the request, checking to determine whether a valid copy of the data exists" as set forth in Claims 1, 9, and 19. In other words, each of the processors and memory would not have to check to determine whether a valid copy of the data exists because that information would already have been determined according to the Examiner. In which case, the arguments set forth by the Examiner would negate the rejection of Claims 1, 9, and 19 as being unpatentable over Van Doren as failing to disclose each and every element recited in the claims.

It also appears that the Official Action may have mistakenly interpreted the language in Claims 1, 9, and 19 as "only the processor or memory having the valid copy returns the valid copy to the requesting processor." This is not what is claimed in Claims 1, 9, and 19. Instead, these claims recite, "only the processor or memory having the valid copy of the data responds to the request." Thus, it is the response to the request and not the return of the valid copy that only the processor or memory having the valid copy of the data performs. Consequently, all of the arguments presented in the Official Action directed to returning the valid copy to the requesting processor do not accurately correspond to the features set forth in Claims 1, 9, and 19.

The arguments continue to state that "the Examiner believes that the operation of returning the valid copy is the action of the response to the request." This statement may be

true with respect to the processor or memory having the valid copy of the requested data. However, this statement in no way pertains to the feature that "only the processor or memory having the valid copy of the data responds to the request." That is, there is nothing in the Examiner's statement to indicate that the other processors or memory that do not have the valid copy do not respond to the request.

At least by virtue of the foregoing arguments, it is respectfully submitted that the assertions contained in the Official Action are misdirected and cannot be construed as being persuasive in maintaining the rejections contained in the Official Action.

Conclusion

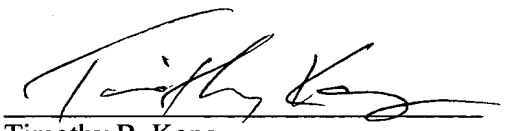
In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please

grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

Fong Pong

Dated: October 14, 2003 By 

Timothy B. Kang
Registration No.: 46,423

MANNAVA & KANG
2930 Langdon Gate Drive
Fairfax, VA 22031
(703) 560-8503
(703) 991-1162 (facsimile)